VDIC ASYNCHRONOUS STATIC RAM

VDSR8M16XS54XX2V12 USER MANUAL

Version :A5

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VDIC-SRAM

HIGH-SPEED 3.3V 512K×16bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR8M16XS54XX2V12 is a high-speed access time, high-density Static Random Access Memory. Manufactured with VDIC Very Dense SIP technology, this SIP module stacks four 4-Mbit SRAM dies employing CMOS process (6-transistor memory cell). It is organized as two independent blocks of 256K× 16bit wide data interface.

Each block can be selected separately with dedicated #CSn.

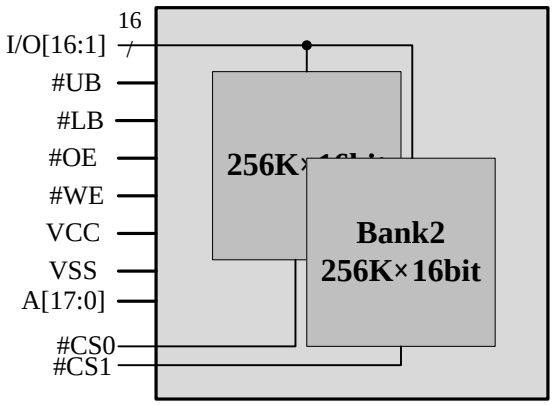
Low interconnect parasitic capacitance of the stacking technology ,by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR8M16XS54XX2V12 is available in 54-pin SOP package.

2 Features

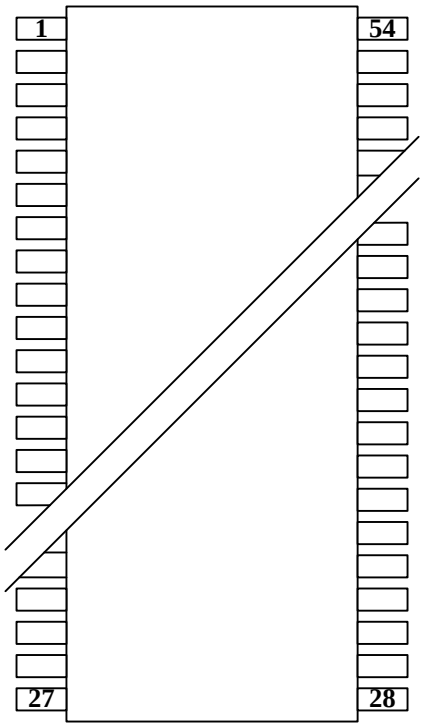
- Single 3.3V±0.3V power supply
- Stack of two 4Mbit SRAM
- Organized as 2 blocks of 256K×16bit
- two independent Chip Select, #CS0 、#CS1、
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Access time: 12ns
- Max. Operating current: 260mA (Max)
- TTL Standby curren(two bank)t: 80mA(Max)
- CMOS standby curren(two bank):10mA(Max)
- No clock or timing strobe required
- 54-lead SOP Type II package

3 Block Diagram



4 Pin Descriptions

Pin Id	Pin #		Pin Id
NC	1	54	**NC**
NC	2	53	**#CS1**
A0	3	52	**A17**
A1	4	51	**A16**
A2	5	50	**A15**
A3	6	49	**#OE**
A4	7	48	**#UB**
#CS0	8	47	**#LB**
I/O1	9	46	**I/O16**
I/O2	10	45	**I/O15**
I/O3	11	44	**I/O14**
I/O4	12	43	**I/O13**
VCC	13	42	**VSS**
VSS	14	41	**VCC**
I/O5	15	40	**I/O12**
I/O6	16	39	**I/O11**
I/O7	17	38	**I/O10**
I/O8	18	37	**I/O9**
#WE	19	36	**NC**
A5	20	35	**A14**
A6	21	34	**A13**
A7	22	33	**A12**
A8	23	32	**A11**
A9	24	31	**A10**
NC	25	30	**NC**
NC	26	29	**NC**
NC	27	28	**NC**



Pin	Name	Function
#CS0	Chip select	Disables or enables memory die1 operation
#CS1	Chip select	Disables or enables memory die2 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation common to all dies
#OE	Output enable	Enables data output common to all dies
#UB	Upper byte select	Latches upper bytes addresses common to all dies
#LB	Lower byte select	Latches lower bytes addresses common to all dies
I/O1 ~ I/O16	Data input/output	Data inputs/outputs 16-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to Vcc+0.5	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

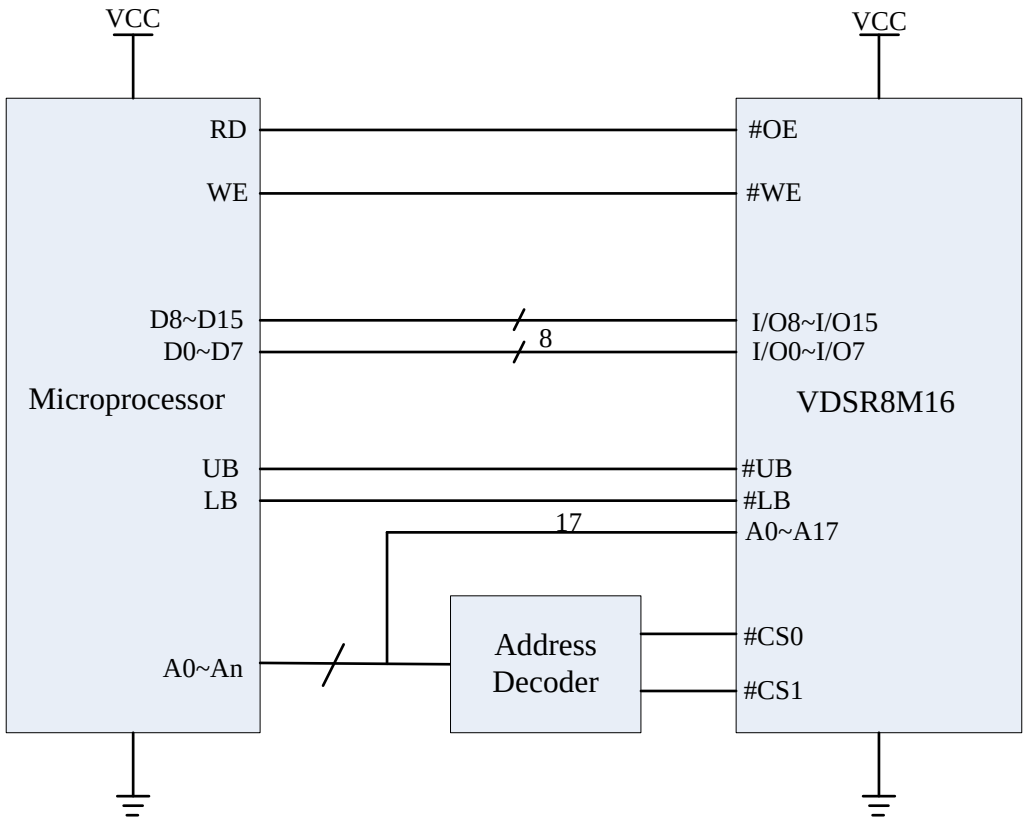
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	-	V_{cc}+0.5	V
Input low voltage	V_{IL}	-0.5	-	0.8	V

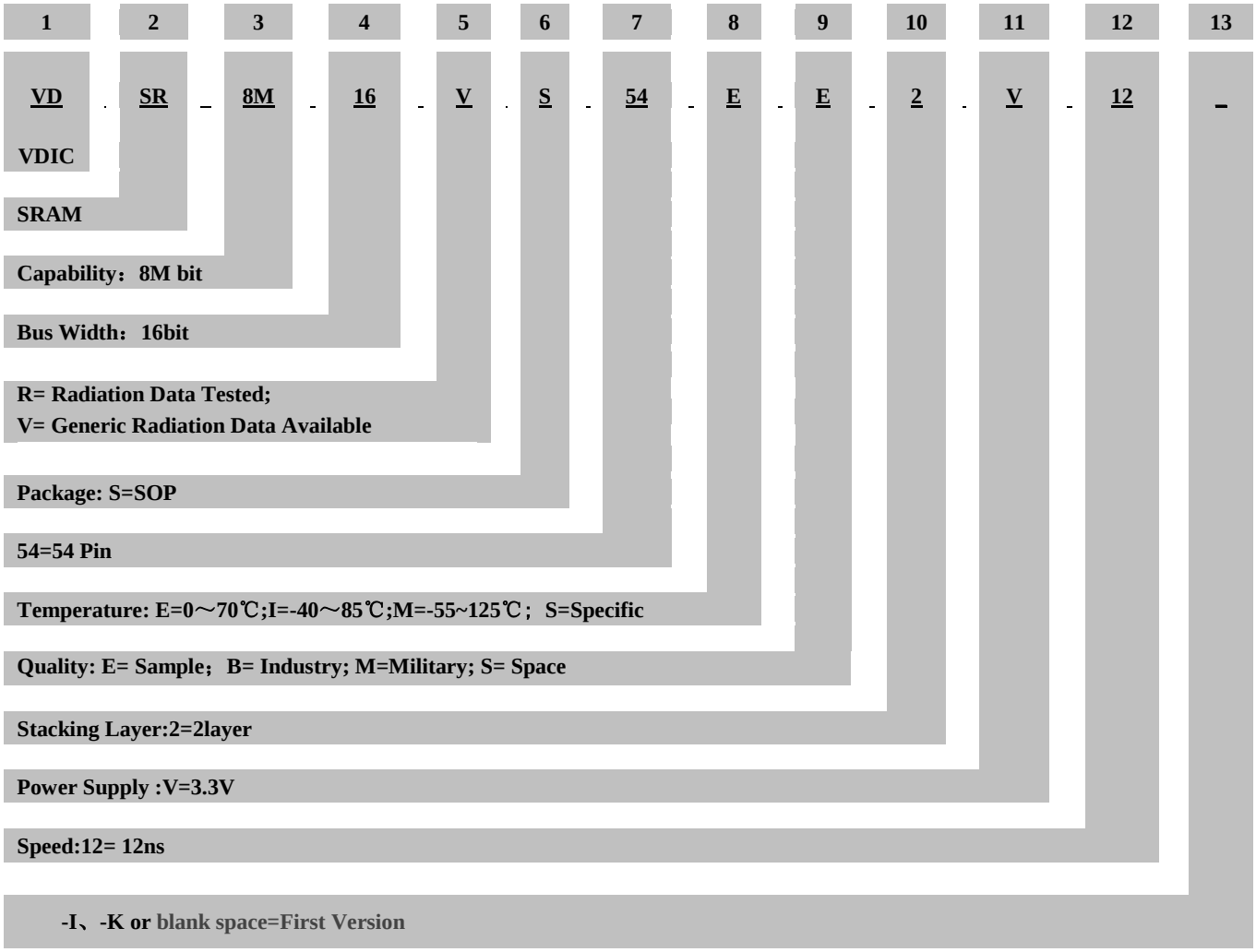
5.3 DC Electrical Characteristics Over The Operating

PARAMETERS	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V_{OL}	V_{cc}=3.6V，I_{OL} = 1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{cc}=3.6V,I_{OH}= -0.5mA	2.4	——	V

6 Typical Application



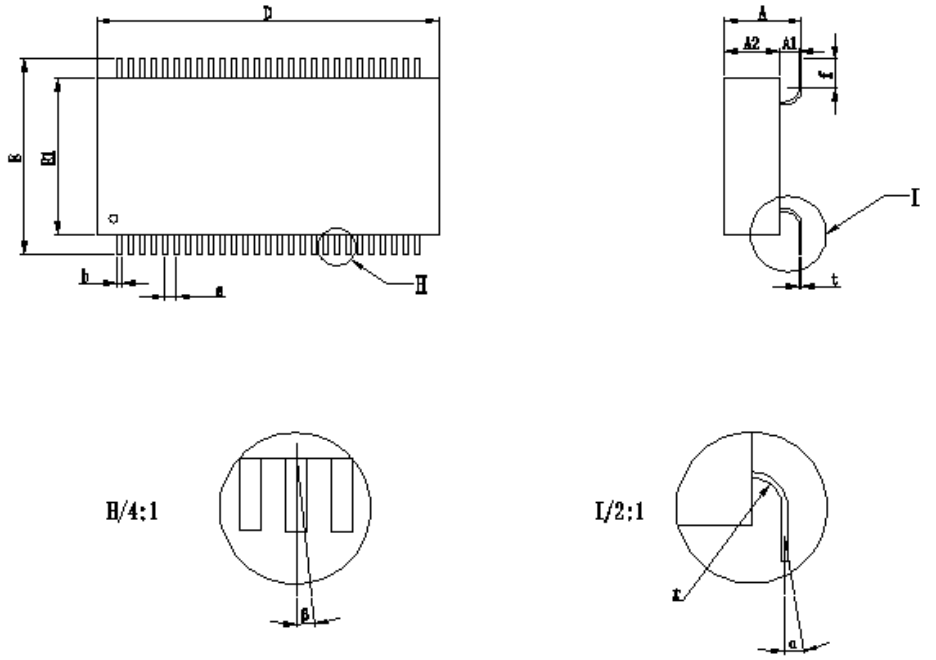
7 Ordering Information



Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR8M16VS54EE2V12	8M	16	-	-	-	SOP54	0 ~ + 70
VDSR8M16VS54IB2V12	8M	16	-	-	-	SOP54	-40 ~ + 85
VDSR8M16VS54MB2V12	8M	16	-	-	-	SOP54	-55 ~ + 125
VDSR8M16VS54MM2V12	8M	16	-	-	-	SOP54	-55 ~ + 125
VDSR8M16RS54MS2V12	8M	16	100	99.8	0.7	SOP54	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 Package Dimensions



	Min	Max
A	5.40	5.80
A2	3.80	4.40
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35±0.03	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1. Unit：mm 2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Apr 13,2018	Modified the PACKAGE DIMENSIONS