

VDIC SYNCHRONOUS DYNAMIC RAM

VD2D8G08XS88XX8U6 USER MANUAL

Version : A0

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VDIC-DDR2 SDRAM

HIGH-SPEED 1.8V 1G x 8bit

SYNCHRONOUS DYNAMIC RAM

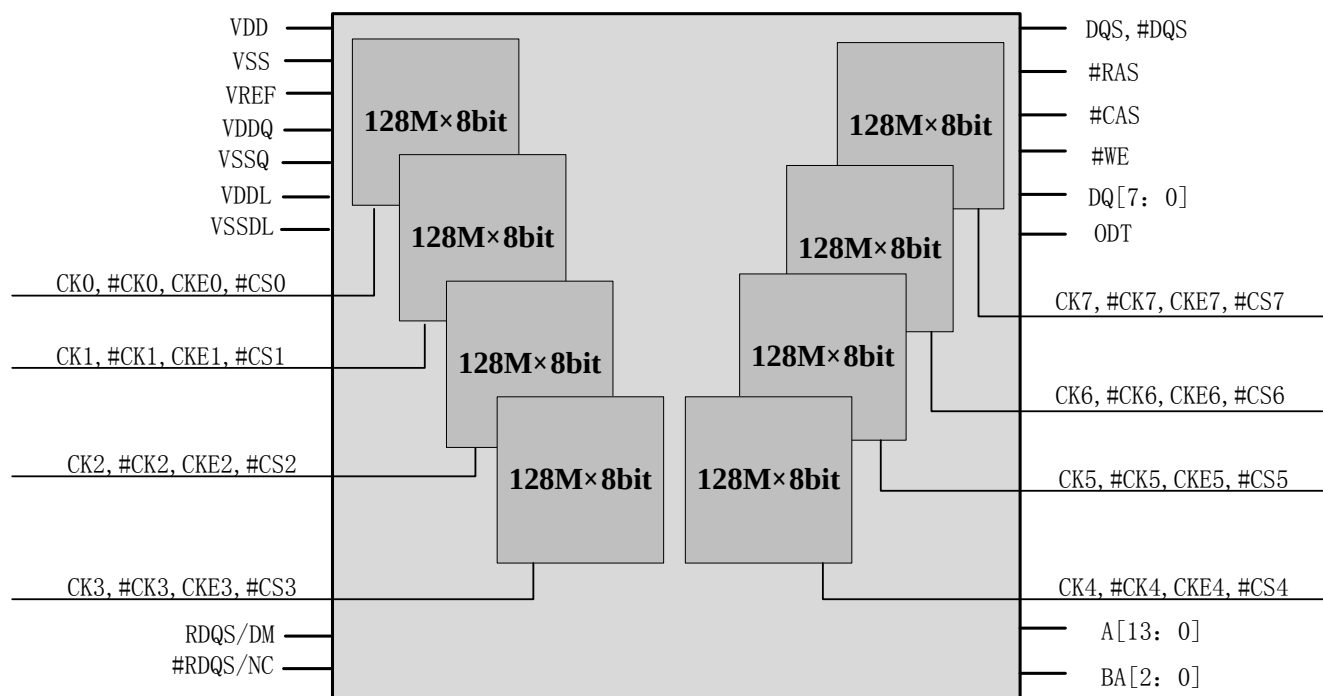
1. DESCRIPTION

The VD2D8G08XS88XX8U6 is a 8G bits DDR2 SDRAM, organized as 1G×8 bit. The device has eight die, each die includes 1Gbit. The device has a 8-bit interface and is selected with specific #CS, CK , #CK and CKE. The device is useful for a variety of high bandwidth, high performance memory system applications.

2. FEATURES

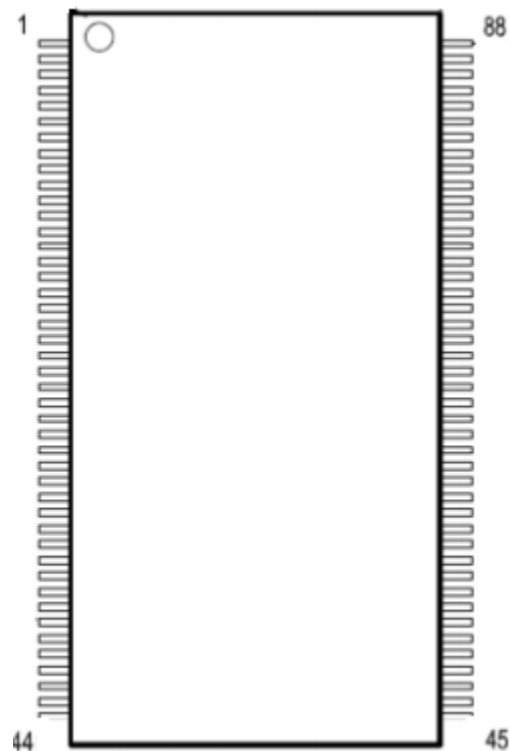
- _Clock frequency up to 400MHz
- _8 internal banks for concurrent operation
- _4-bit prefetch architecture
- _Programmable CAS Latency: 3, 4, 5, 6 and 7
- _Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6
- _Write Latency = Read Latency-1
- _Programmable Burst Sequence: Sequential or Interleave
- _Programmable Burst Length: 4 and 8
- _Automatic and Controlled Precharge Command
- _Power Down Mode
- _Auto Refresh and Self Refresh
- _Refresh Interval: 7.8 s (8192 cycles/64 ms)
- _ODT (On-Die Termination)
- _Weak Strength Data-Output Driver Option
- _Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- _On-Chip DLL aligns DQ and DQs transitions with CK transitions
- _DQS# can be disabled for single-ended data strobe
- _Read Data Strobe supported (x8 only)
- _Differential clock inputs CK and CK#
- _VDD and VDDQ = 1.8V ± 0.1V
- _PASR (Partial Array Self Refresh)
- _SSTL_18 interface
- _tRAS lockout support

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Pin Id	Pin#		Pin Id
VSSQ	1	45	VDD
RDQS/DM	2	46	NC
#RDQS/NC	3	47	ODT
VDDQ	4	48	A11
DQ6	5	49	A13
DQ1	6	50	A8
VSSQ	7	51	A6
DQ4	8	52	A4
VDDQ	9	53	A2
DQ3	10	54	A0
VDDL	11	55	VSS
VREF	12	56	#CK7
#WE	13	57	CK7
CKE3	14	58	VDD
CKE2	15	59	#CK6
CKE1	16	60	CK6
CKE0	17	61	VSS
#RAS	18	62	#CK5
BA0	19	63	CK5
BA2	20	64	VDD
BA1	21	65	#CK4
VSS	22	66	CK4
A10	23	67	VSS
A1	24	68	#CK0
A3	25	69	CK0
A5	26	70	VDD
A12	27	71	#CK1
A7	28	72	CK1
A9	29	73	VSSDL
VDD	30	74	#CK2
#CAS	31	75	CK2
#CS3	32	76	VSS
#CS2	33	77	#CK3
#CS1	34	78	CK3
#CS0	35	79	VDDQ
#CS4	36	80	DQ2
#CS5	37	81	DQ5
#CS6	38	82	VSSQ
#CS7	39	83	DQ0
CKE4	40	84	DQ7
CKE5	41	85	VDDQ
CKE6	42	86	#DQS
CKE7	43	87	DQS
VSS	44	88	VSSQ



Symbol	Description
CK0~CK7, #CK0~#CK7	Input clocks
CKE0~CKE7	Clock enable
#CS0~#CS7	Chip Select
#RAS, #CAS, #WE	Command control inputs
A[13:0]	Address
BA[2:0]	Bank Address
DQ[7:0]	I/O
DQS , #DQS	Data Strobe
DM	Input data mask
ODT	On Die Termination Enable
VDD	Supply voltage
VSS	Ground
VREF	Reference voltage
NC	Not connected

Note: VDDL and VSSDL are power and ground for the DLL.

5. DC OPERATING CONDITIONS

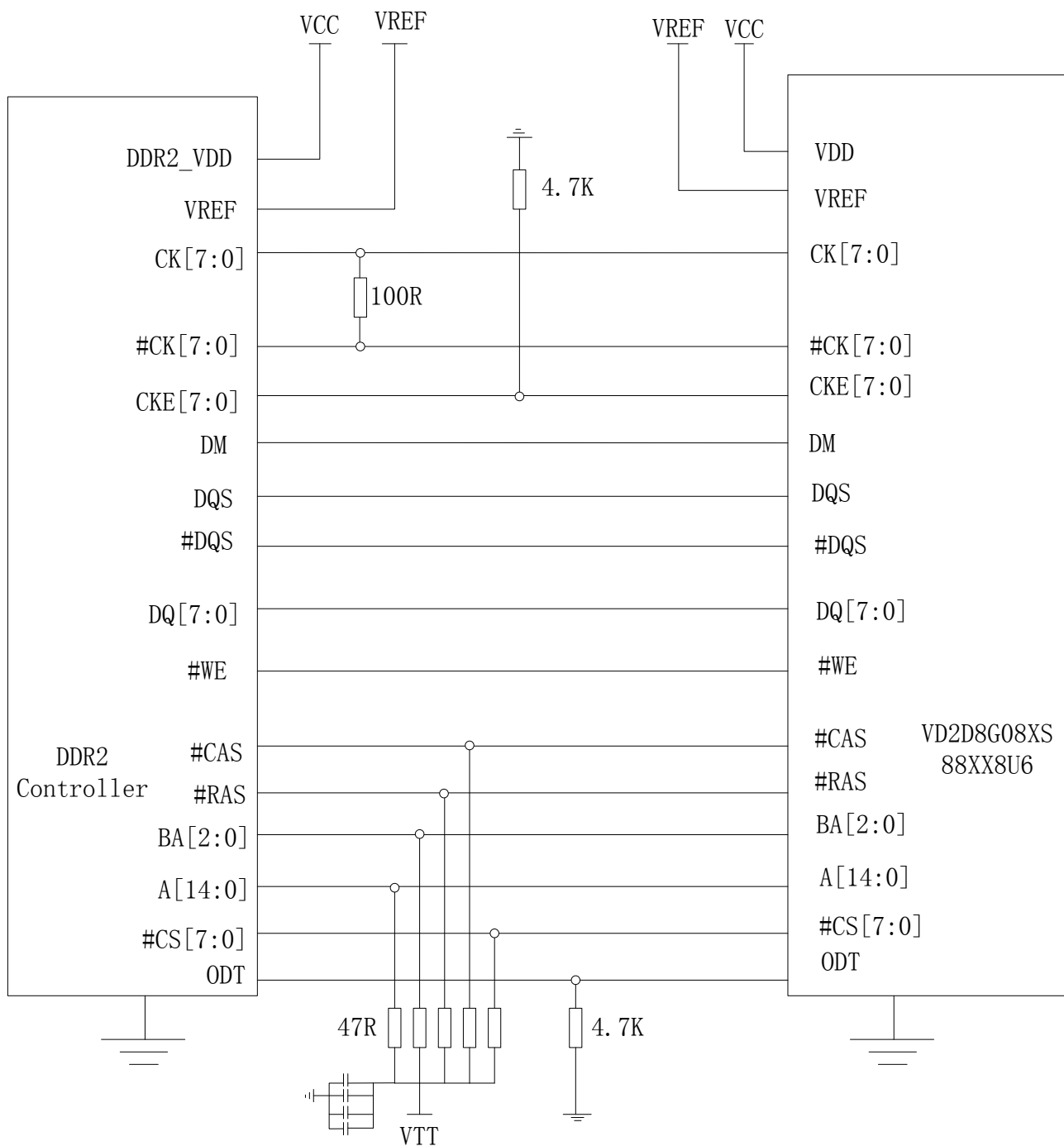
5.1. ABSOLUTE MAXIMUM DC RATINGS

Symbol	Parameter	Rating	Unit
VDD	Voltage on VDD pin relative to Vss	-1.0 to 2.3	V
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 to 2.3	V
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 to 2.3	V
Vin, Vout	Voltage on any pin relative to Vss	- 0.5 to 2.3	V
T _{OPR}	Operating Temperature Range	-40~ +105	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
P _D	Packaging power dissipation	1	W

5.2. Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V
VREF	Input Reference Voltage	$0.49 \cdot VDDQ$	$0.50 \cdot VDDQ$	$0.51 \cdot VDDQ$	V
VIH	High-level input voltage DC	$VREF + 0.125$	—	$VDDQ + 0.3$	V
VIL	Low-level input voltage DC	-0.3	—	$VREF - 0.125$	V

6. TYPICAL APPLICATION



7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>2D</u>	<u>8G</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>88</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>U</u>	<u>6</u>	<u>-</u>
VDIC												
DDR2												
Capability: 8G bit												
Bus Width: 8bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: B=BGA; S=SOP												
88=88 Pin												
Temperature::E=0~70℃;I=-40~85℃;S=Specific												
Quality: E= Sample; B= Industry; S= Space												
Stacking Layer:8=81ayer												
Power Supply :U=1.8V												
Speed:6=400MHz												
-I、-K or blank space=First Version												

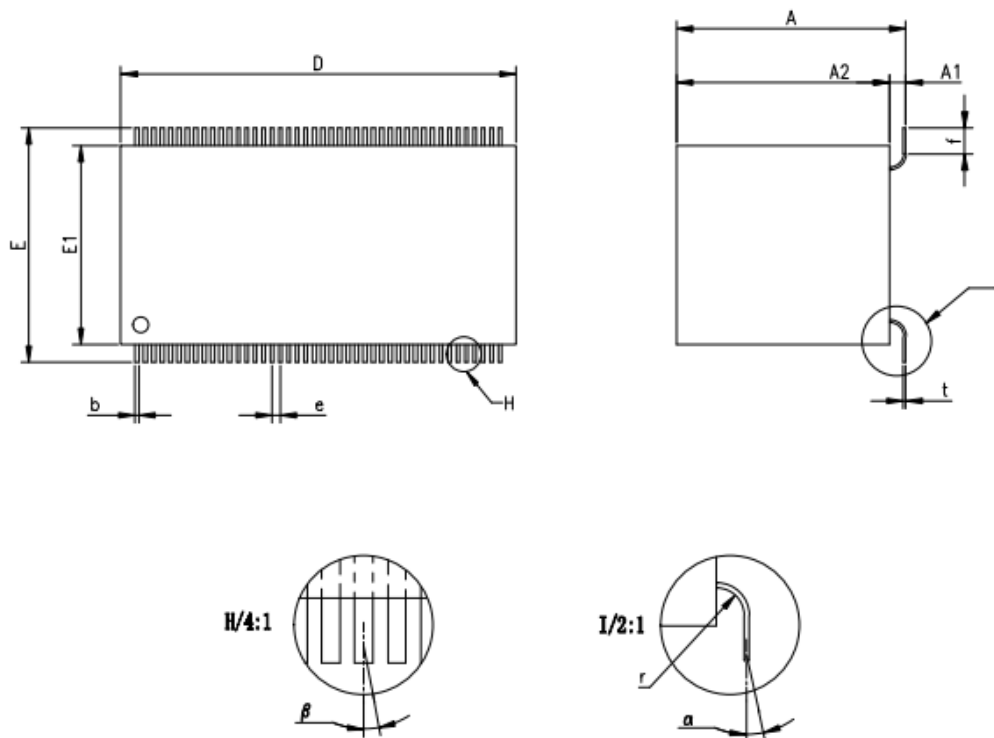
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VD2D8G08VS88EE8U6	8G	8	-	-	-	-	0 ~ + 70
VD2D8G08VS88IB8U6	8G	8	-	-	-	-	-40 ~ + 85
VD2D8G08VS88IS8U6	8G	8	-	-	-	-	-40 ~ + 85
VD2D8G08RS88SS8U6	8G	8	100	>68	0.8	-	-40 ~ + 105

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8. PACKAGE DIMENSIONS



	Min	Max
A	17.40	17.90
A2	15.90	16.50
D	30.20	30.60
E	17.70	18.10
E1	15.10	15.50
f	2.0	
b	0.3	
e	0.65	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE : 1.U int : mm		
2. A1= A - A2		

9. REVISION HISTORY

Revision	Date	Description of Change
A0	Aug 9,2018	First Created