

VDIC ASYNCHRONOUS STATIC RAM

VDSR16M16XS54XX4C12 USER MANUAL

Version : B0

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Contents

1	Description	1
2	Features	1
3	Block Diagram	2
4	Pin Descriptions	2
5	Command Operation	3
5.1	Absolute Maximum Ratings.....	3
5.2	Recommended DC Operating Conditions.....	3
5.3	DC Electrical Characteristics Over The Operating.....	4
6	Typical Application.....	4
7	Ordering Information.....	5
8	Package Dimensions.....	6
9	REVISION HISTORY	7

VDIC-SRAM

HIGH-SPEED 1M×16bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR16M16XS54XX4C12 is a high-speed access time, high-density Static Random Access Memory. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is organized as four independent blocks of 256Kx16bit wide data interface. Each block can be selected separately with dedicated #CSn.

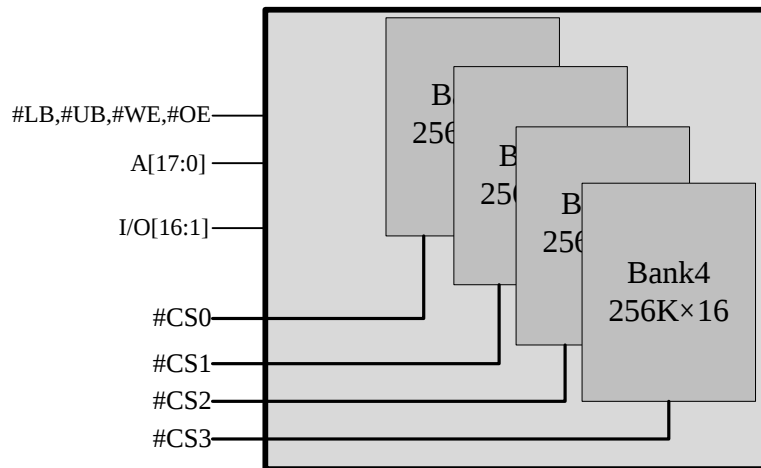
Low interconnect parasitic capacitance of the stacking technology , by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR16M16XS54XX4C12 is available in 54-pin SOP package.

2 Features

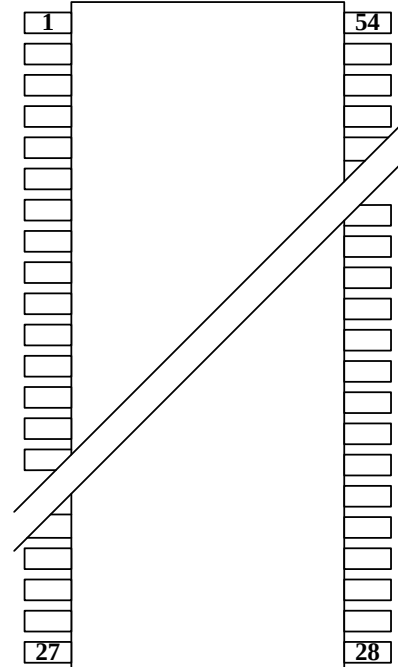
- Single 5V supply:5.0V±0.5
- Access time: 15ns
- Completely static memory
- No clock or timing strobe required
- Equal Access and Cycle times
- All inputs and outputs directly TTL compatible
- Operating current: 280mA (Max)
- TTL Standby current: 160mA(Max)
- CMOS standby current:20mA(Max)
- Stack of four 4Mbit SRAM
- Organized as 4 blocks of 256Kx16bit
- Four independent Chip Select, #CS0、 #CS1、 #CS2、 #CS3
- Center Power/Ground pin Configuration
- 54-lead SOP Type II package

3 Block Diagram



4 Pin Descriptions

Pin Id	Pin #		Pin Id
NC	1	54	#CS3
NC	2	53	#CS1
A0	3	52	A17
A1	4	51	A16
A2	5	50	A15
A3	6	49	#OE
A4	7	48	#UB
#CS0	8	47	#LB
I/O1	9	46	I/O16
I/O2	10	45	I/O15
I/O3	11	44	I/O14
I/O4	12	43	I/O13
VCC	13	42	VSS
VSS	14	41	VCC
I/O5	15	40	I/O12
I/O6	16	39	I/O11
I/O7	17	38	I/O10
I/O8	18	37	I/O9
#WE	19	36	NC
A5	20	35	A14
A6	21	34	A13
A7	22	33	A12
A8	23	32	A11
A9	24	31	A10
NC	25	30	#CS2
NC	26	29	NC
NC	27	28	NC



Pin	Name	Function
#CS0	Chip select	Disables or enables memory bank operation
#CS1	Chip select	Disables or enables memory bank 2 operation

Pin	Name	Function
#CS2	Chip select	Disables or enables memory bank 3 operation
#CS3	Chip select	Disables or enables memory bank 4 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all banks
#OE	Output enable	Enables data output command to all banks
#UB	Upper byte select	Latches upper bytes data(I/O[16:9]) to all banks
#LB	Lower byte select	Latches lower bytes data (I/O[8:1]) to all banks
I/O1 ~ I/O16	Data input/output	Data inputs/outputs 16-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V _{SS}	V _{IN}	-0.5 to V _{CC} +0.5	V
Power Dissipation	P _D	1.5	W
Operating Temperature Range	T _{OPR}	-55 to +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

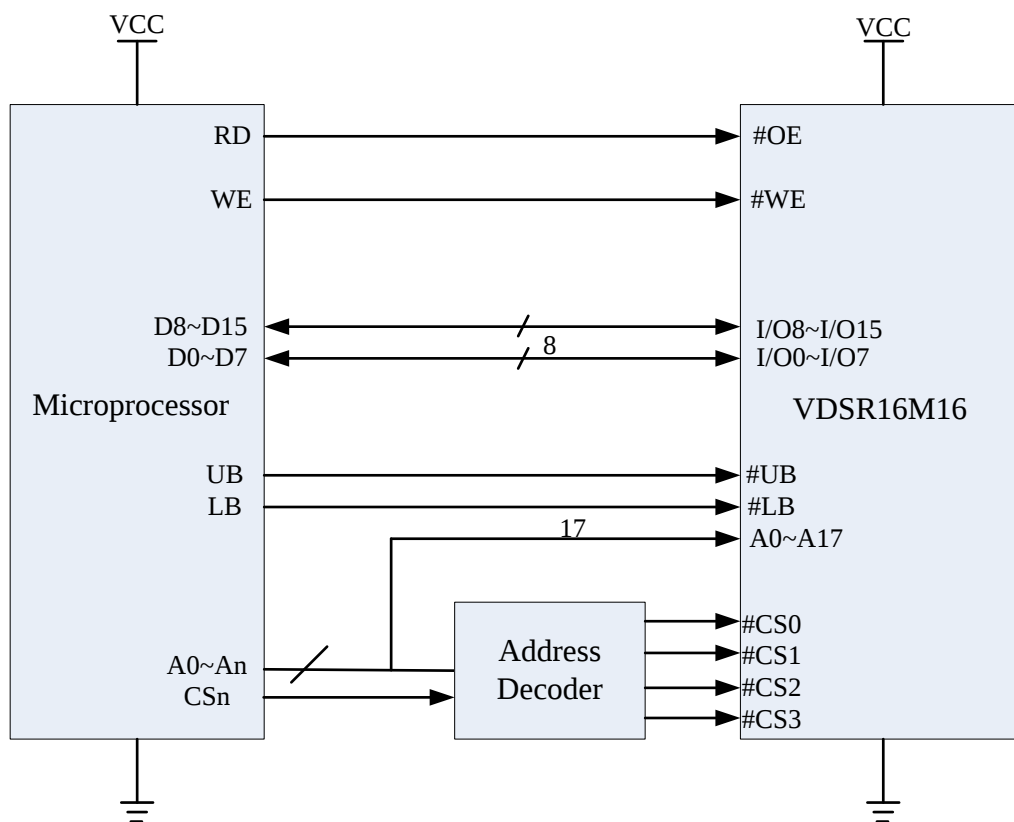
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2	—	V _{CC} +0.5	V
	V _{IL}	-0.5	—	0.8	V

5.3 DC Electrical Characteristics Over The Operating

PARAMETERS	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V_{OL}	$V_{CC}=4.5V$, $I_{OL} = 1mA$	—	0.4	V
Output voltage high level	V_{OH}	$V_{CC}=4.5V, I_{OH}= -0.5mA$	2.4	—	V

6 Typical Application



7 Ordering Information

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>SR</u>	<u>16M</u>	<u>16</u>	<u>V</u>	<u>S</u>	<u>54</u>	<u>E</u>	<u>E</u>	<u>4</u>	<u>C</u>	<u>12</u>	<u>-</u>
VDIC												
SRAM												
Capability: 16M bit												
Bus Width: 16bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: S=SOP												
54=54 Pin												
Temperature: E=0~70℃;I=-40~85℃;M=-55~125℃ ; S=Specific												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer:4=4layer												
Power Supply :C=5.0V												
Speed:12= 12ns												
-I、 -K or blank space=First Version												

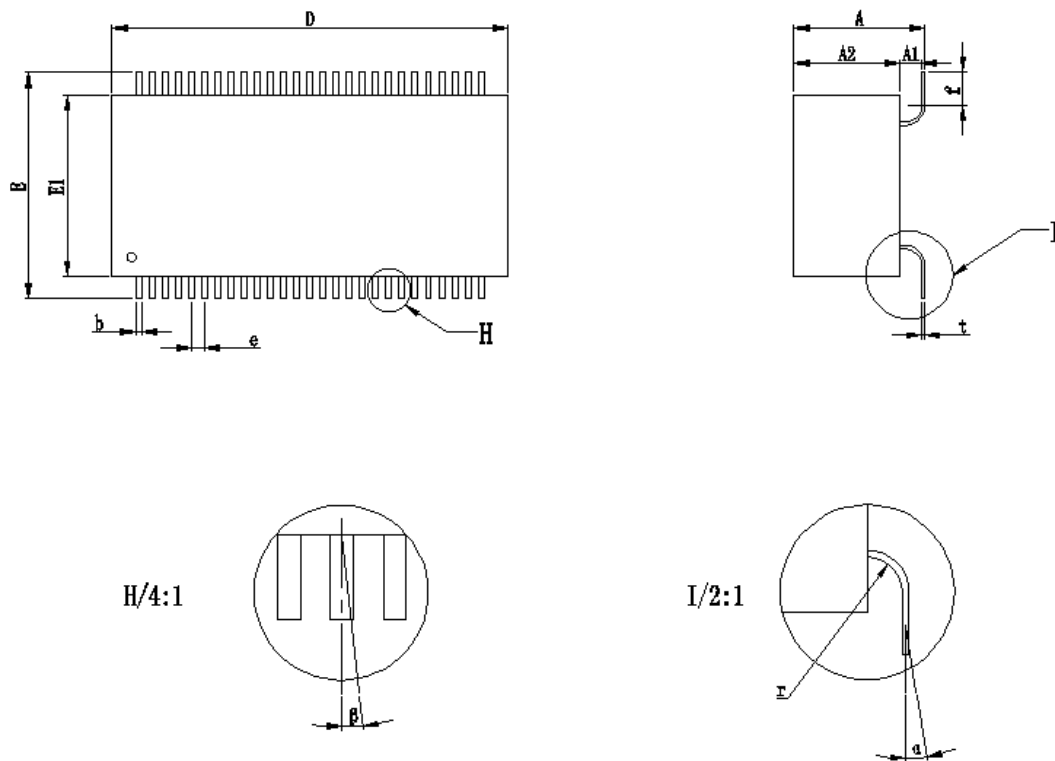
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSR16M16VS54EE4C12	16M	16	-	-	-	SOP54	0 ~ + 70
VDSR16M16VS54IB4C12	16M	16	-	-	-	SOP54	-40 ~ + 85
VDSR16M16VS54MB4C12	16M	16	-	-	-	SOP54	-55 ~ + 125
VDSR16M16VS54MM4C12	16M	16	-	-	-	SOP54	-55 ~ + 125
VDSR16M16RS54MS4C12	16M	16	100	99.8	0.7	SOP54	-55 ~ + 125

¹ TID: Total Dose (Krads(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8 Package Dimensions



	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.0	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE : 1. Unit : mm		
2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Apr 13,2018	Modified the PACKAGE DIMENSIONS
B0	Oct 18,2018	Revising pin descriptions